

REMARKS

Claims 1-2, 7-8, 15, 17-27 and 29-31 are pending.

Claims 3-6, 9-14, 16 and 28 have been cancelled.

Claims 32-36 have been added.

In the Office Action dated January 23, 2009, claims 1 and 7 were rejected on the ground of nonstatutory obviousness-type double patenting over claims 1 and 14, respectively, of U.S. Patent No. 7,093,147 in view of U.S. Patent 7,093,147 (Yamaji); claims 1, 2, 7-8, 15, 17-19, 22-23, 25-28, and 30-31 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Publication No. 2003/0110012 (Orenstien) in view of U.S. Patent No. 6,332,178 (Dean); claim 24 was rejected under 35 U.S.C. § 103(a) as unpatentable over Orenstien in view of Dean and further in view of U.S. Patent No. 6,986,141 (Diepstraten); and claims 1, 2, 7-8, 15, 17-19, 22-28, and 30-31 were rejected under 35 U.S.C. § 103(a) as unpatentable over Orenstien in view of Yamaji.

Claims 20, 21, and 29 were objected to but were indicated as containing allowable subject matter. Claims 20 and 29 have been amended from dependent form to independent form. The language of claims 20 and 29 has been amended to improve their form as well as to broaden the scope of these claims. However, it is believed that claims 20 and 29 are still in condition for allowance.

Double Patenting Rejection

Claims 1 and 7 were rejected based on the ground of nonstatutory obviousness-type double patenting over claims 1 and 14, respectively, of U.S. Patent No. 7,093,147 in view of Yamaji.

In view of the amendment of present independent claim 1, it is believed that the double-patenting rejection of present claim 1 over claim 1 of the '147 Patent and Yamaji has been rendered moot. Claim 1 of the '147 Patent and Yamaji, even if combined, would not provide any teaching or hint of a performance measurement and transfer mechanism to move a plurality of executing computer processing jobs amongst a plurality of computer processor cores by matching requirements of a plurality of executing computer processing jobs to processing capabilities of the computer processor

cores. Therefore, present claim 1 is non-obvious over claim 1 of the '147 Patent in view of Yamaji.

It is respectfully submitted that present independent claim 7 is also non-obvious over claim 14 of the '147 Patent in view of Yamaji. It is respectfully submitted that the hypothetical combination of claim 14 of the '147 Patent and Yamaji would not have provided a teaching or hint of at least the following element of claim 7: "transferring individual ones of a plurality of computer processing jobs amongst targeted ones of said plurality of computer processor cores based on the throughput metric." Although Yamaji refers to a "throughput coefficient," it is noted that this throughput coefficient is not used for transferring computer processing jobs amongst computer processor cores. Yamaji is concerned with determining whether a new job is to be started on a processor based on a measured workload. Therefore, even if claim 14 of the '147 Patent and Yamaji were to be hypothetically combined, this hypothetical combination would not have led to the "transferring" element of present claim 7, in combination with the other elements of present claim 7. Therefore, present claim 7 is non-obvious over claim 14 of the '147 Patent in view of Yamaji.

Withdrawal of the double patenting rejection is respectfully requested.

Rejections Under 35 U.S.C. § 103

Independent claim 1 was rejected as purportedly obvious over Orenstien in view of Dean. It is respectfully submitted that claim 1 is non-obvious over the cited references.

To make a determination under 35 U.S.C. § 103, several basic factual inquiries must be performed, including determining the scope and content of the prior art, and ascertaining the differences between the prior art and the claims at issue. *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 U.S.P.Q. 459 (1965). Moreover, as held by the U.S. Supreme Court, it is important to identify a reason that would have prompted a person of ordinary skill in the art to combine reference teachings in the manner that the claimed invention does. *KSR International Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1741, 82 U.S.P.Q.2d 1385 (2007).

Orenstien discloses a monitor that receives power consumption information from processing units and analyzes whether power consumption between the processing units is sufficient uneven to justify the overhead of re-allocating processes to different processing units. Orenstien, ¶ [0020]. In ¶ [0021], Orenstien discloses that process rotation between processing units may be based on a power consumption metric and/or to level the load between the processors. However, re-allocating processes among processing units based on power consumption or to even the load is quite different from moving a plurality of executing computer processing jobs among a plurality of computer processor cores by matching requirements of the plurality of executing computer processing jobs to processing capabilities of the computer processor cores. The metrics of interest in Orenstien are a power consumption metric and/or an uneven load metric. The concept of matching requirements of computer processing jobs to processing capabilities of computer processor cores does not exist in Orenstien.

Similarly, Dean also does not provide any teaching or hint of the claimed subject matter discussed above that is missing from Orenstien. Dean describes computing latency-based statistics with respect to processing a memory transaction. Dean, 12:28-35. Dean discloses that in a non-uniform memory access multiprocessor system, data that is frequently accessed by a processor can be moved to a region of the memory system associated with that processor so that the data can be accessed more quickly by the processor. *Id.*, 12:66-13:6. Dean provides no hint of moving computer processing jobs amongst computer processor cores by matching requirements of the computer processing jobs to processing capabilities of the computer processor cores.

In view of the foregoing, it is respectfully submitted that since the hypothetical combination of Orenstien and Dean would not have led to the claimed subject matter, the obviousness rejection is defective for at least this reason.

Moreover, in view of the significant differences between Orenstien/Dean and the present claimed subject matter, it is respectfully submitted that a person of ordinary skill in the art would not have been prompted to combine the teachings of Orenstien and Dean to achieve the claimed subject matter. Orenstien relates to re-allocating processes among processing units based on a power consumption metric or to level the load between the

processing units. Dean relates to moving data to a region of a memory system associated with the processor so that the processor can more quickly access the data. A person of ordinary skill in the art, based on such teachings, would have found no reason to combine Orenstien and Dean to perform moving computer processing jobs amongst computer processor cores by matching requirements of the computer processing jobs to processing capabilities of the computer processor cores.

The obviousness rejection of claim 1 over Orenstien and Dean is therefore defective for this additional reason.

Independent claim 1 was also rejected as purportedly obvious over Orenstien and Yamaji. It is respectfully submitted that the hypothetical combination of Orenstien and Yamaji also would not have provided any teaching or hint of the subject matter of claim 1. As explained above, Orenstien does not disclose the “performance measurement and transfer mechanism” element of claim 1. Yamaji describes use of a throughput coefficient to determine whether a new job can be started on a processor based on a current workload of the processor. Yamaji, Abstract. This teaching of Yamaji has nothing to do with assigning computer processing jobs amongst computer processor cores by matching requirements of computer processing jobs to processing capabilities of computer processor cores.

Thus, the hypothetical combination of Orenstien and Yamaji would clearly not have led to the subject matter of claim 1. Moreover, in view of the significant difference between the claimed subject matter and the teachings of Orenstien and Yamaji, it is respectfully submitted that a person of ordinary skill in the art would not have been prompted to combine the reference teachings to provide moving computer processing jobs amongst computer processor cores by matching requirements of computer processing jobs to processing capabilities of computer processor cores.

In view of the foregoing, the obviousness rejection of claim 1 over Orenstien and Yamaji is also clearly defective.

Independent claim 25 is similarly allowable over either Orenstien/Dean or Orenstien/Yamaji.

Independent claim 7 is also non-obvious over Orenstien and Dean. Claim 7 recites a method for operating multiple processor cores, comprising:

- obtaining a throughput metric that identifies throughput achieved by a plurality of computer processor cores as a function of workloads running on said computer processor cores, wherein the plurality of computer processor cores are on a single semiconductor die, in which at least two computer processor cores differ in processing capability, and wherein the computer processor cores execute the same instruction set; and
- transferring individual ones of said plurality of computer processing jobs amongst targeted ones of a plurality of computer processor cores based on the throughput metric.

As conceded by the Office Action, Orenstien fails to disclose obtaining a throughput metric that identifies throughput achieved by computer processor cores as a function of workloads running on the computer processor cores. 1/23/2009 Office Action at 8. The Office Action cited Dean as purportedly disclosing this claimed feature. *Id.* As explained above, Dean relates to moving data to a memory system of a processor so that the processor can access the data more quickly. Dean has nothing to do with obtaining a throughput metric as defined by claim 7, and transferring individual ones of the computer processing jobs amongst targeted ones of the computer processor cores based on such throughput metric.

Therefore, the hypothetical combination of Orenstien and Dean clearly would not have disclosed or hinted at the subject matter of claim 7.

Moreover, a person of ordinary skill in the art would not have been prompted to apply the teachings of Dean to Orenstien to achieve the claimed subject matter. Moving data to different memory systems so that the corresponding processors can access the data more quickly, as taught by Dean, has nothing to do with re-allocating processes among processing units based on power consumption or uneven loading, as taught by Orenstien.

In view of the foregoing, the obviousness rejection of claim 7 over Orenstien and Dean is clearly defective.

It is respectfully submitted that claim 7 is also non-obvious over Orenstien and Yamaji. Yamaji was cited by the Office Action as purportedly disclosing the "throughput

metric" of claim 7 that was conceded to be missing from Orenstien. 1/23/2009 Office Action at 15. However, it is noted that although Yamaji discloses determining whether a new job is to be assigned to a processor based on the present workload of the processor, Yamaji provides no teaching or hint of transferring individual ones of computer processing jobs amongst targeted ones of computer processor cores based on an obtained throughput metric that identifies throughput achieved by the computer processor cores as a function of workloads running on the computer processor cores. Thus, the hypothetical combination of Orenstien and Yamaji would not have led to the subject matter of claim 7.

In view of the foregoing, the obviousness rejection of claim 7 is defective.

Dependent claims, including newly added dependent claims 32-36, are allowable for at least the same reasons as corresponding independent claims.

Allowance of all claims is respectfully requested.

The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account No. 08-2025 (200210109-1).

Respectfully submitted,



Date: April 23, 2009

Dan C. Hu
Registration No. 40,025
TROP, PRUNER & HU, P.C.
1616 South Voss Road, Suite 750
Houston, TX 77057-2631
Telephone: (713) 468-8880
Facsimile: (713) 468-8883